AMT630A

Video Display Controller

(Product Specification)

Version 1.1

2015.01

Revision Record:

Date	Revision	Modification Description
2014-10-8	V1.0	Initial Version
2015-01-05	V1.1	Adjust Electrical Characteristics

1. General Description

AMT630A is a highly integrated video control SoC with Digital LCD/TFT panel displaying controller and could support parallel RGB panel, sRGB panel, ITU656 panel, digital TCON and CPU panel. AMT630A integrates a video decoder and a digital TFT-LCD Panel Control. It accepts analog NTSC / PAL / SECAM CVBS signals from TV tuner, DVD, or VCR sources, including weak and distorted signals. Automatic gain control (AGC) and 9-bit 1-channel A/D converters provide high resolution video quantization, with automatic video source and mode detection. User can easily switch and adjust variety of signal source. Multiple internal adaptive PLL could precisely extract pixel clock from video source and perform sharp-and-keen color demodulation. Build-in line buffer supports adaptive 2-D comb-filter, 2-D sharpening, and synchronization stable in a condense manner. Build-in On Screen Display (OSD) module is very flexiable and easy programming. AMT630A is perfect excellent efficiency for a low-cost Price and small-area PCB solution.

2. Features

Video Decoder

- Composite video signal(CVBS) input; Multiple standards supported: NTSC and NTSC-Japan; PAL (B, D, G, H, I, M, N, etc.); SECAM;
- Three analog inputs: 3xCVBS
- Digital AGC,ACC
- 9-Bit 1-Channel A/D converters with fixed sampling clock
- Only one crystal (27 MHz) required for all standards
- Internal PLL to generate video clock
- Adaptive 2-D comb filter for luminance and chrominance separation
- Precise chrominance demodulation
- Internal buffers for video stability control
- Video noise reduction

Video Enhancement

- Frequency directive sharpening
- Brightness, contrast, saturation, and Tint Adjustments

- Black-Level Extension and White-Level Extension
- Digital Chrominance Transient Improvement(DCTI) and Digital Luminance Transient Improvement(DLTI)
- 3-channel gamma curve adjustment
- Green level enhancement
- Auto contrast adjustment
- Auto chrominance adjustment

Scaling Engine

- Support Digital panel with the resolution of 480x240, 640x240, 520x288, 800x480, 800x600,1024x768, and more
- Support horizontal panorama scaling
- Support vertical panorama scaling

OSD Block

- Built-in 418-character font ROM (Including special font characters)
- Dynamic OSD font RAM------4096x16 bytes
- 16 colors palette, support 5 OSD windows
- Support 16 color bitmap
- Blending with OSD content and video
- Support 3 windows Blinking and highlight function
- Support horizontal and vertical mirror image around function

Interface

- Build-in parallel RGB panel, sRGB panel, digital TCON panel and CPU panel interfaces
- Digital RGB Independent Output Line-Inversion, Offset Control
- 8-Bit/10-Bit CCIR 656 Digital Video Output Format Support
- I2C-BUS interface (slave)

MCU

- Instruction fully compatible with industry standard 803x/805x, fully static synchronous design
- High performance with 4 clock cycles per instruction cycle, up to 27MHz clock speed

- Build-in 3 channels 12Bit ADC for serial key or other analog input
- Supports 13 standard interrupt sources include external interrupt, 3 Timer, watchdog etc
- Programmable I/O ports (GPIO)
- I2C-BUS interface (slave mode)
- Hardware remoter decoder and encoder, support NEC and RC-5 IR protocol

Peripheral

- Build-in MCU(8052) & SPI flash interface
- Build-in 12 Bit SAR ADC
- Build-in display PLL
- Build-in LDO for 1.2v core power
- 3.3V power supply

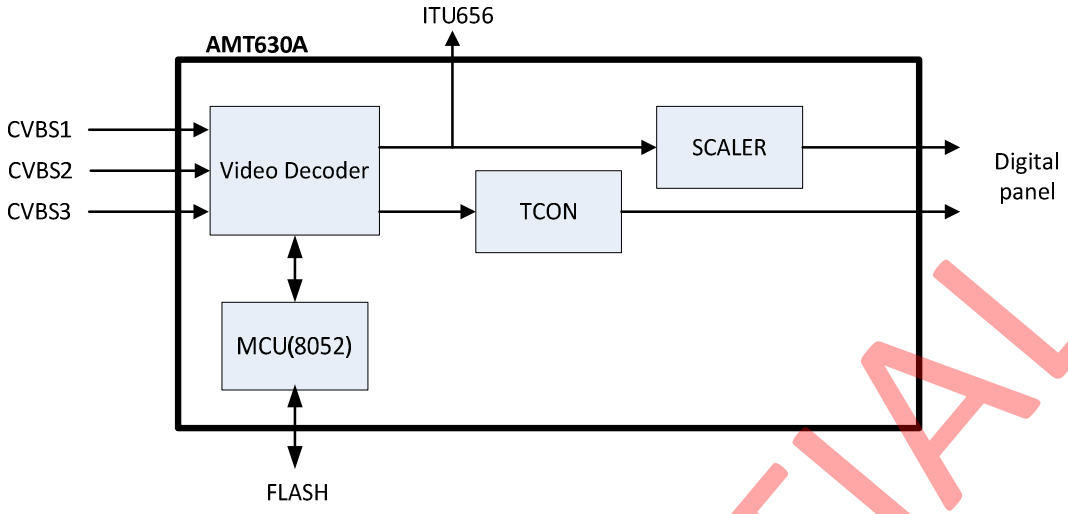
Package

- LQFP 64 Pin Package

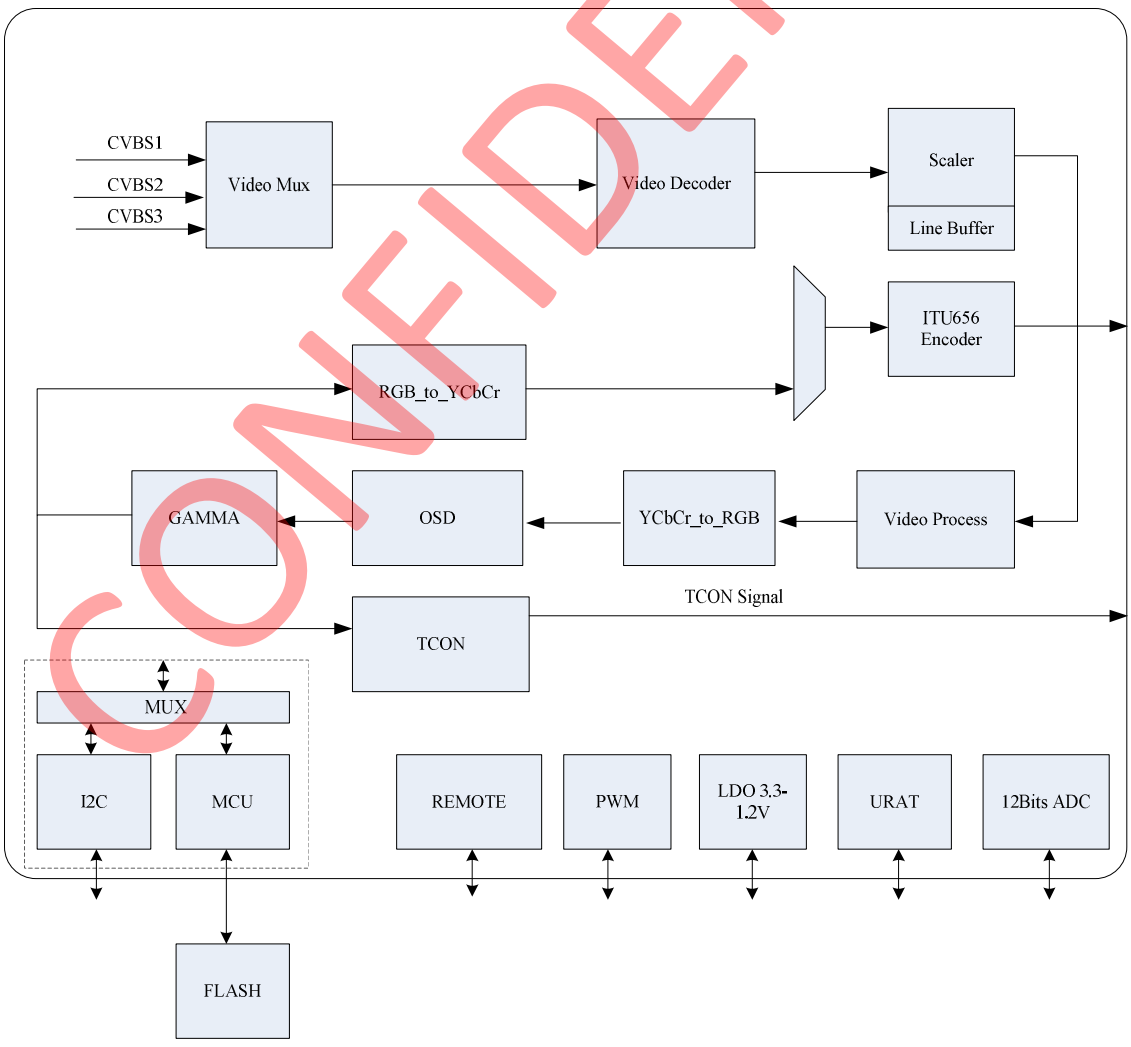
3. Application Field

- Car Reversing Monitor
- Visible Door Monitor
- Portable DVD / TV
- Small to medium sized LCD TV
- Other application using analog panel as the display unit

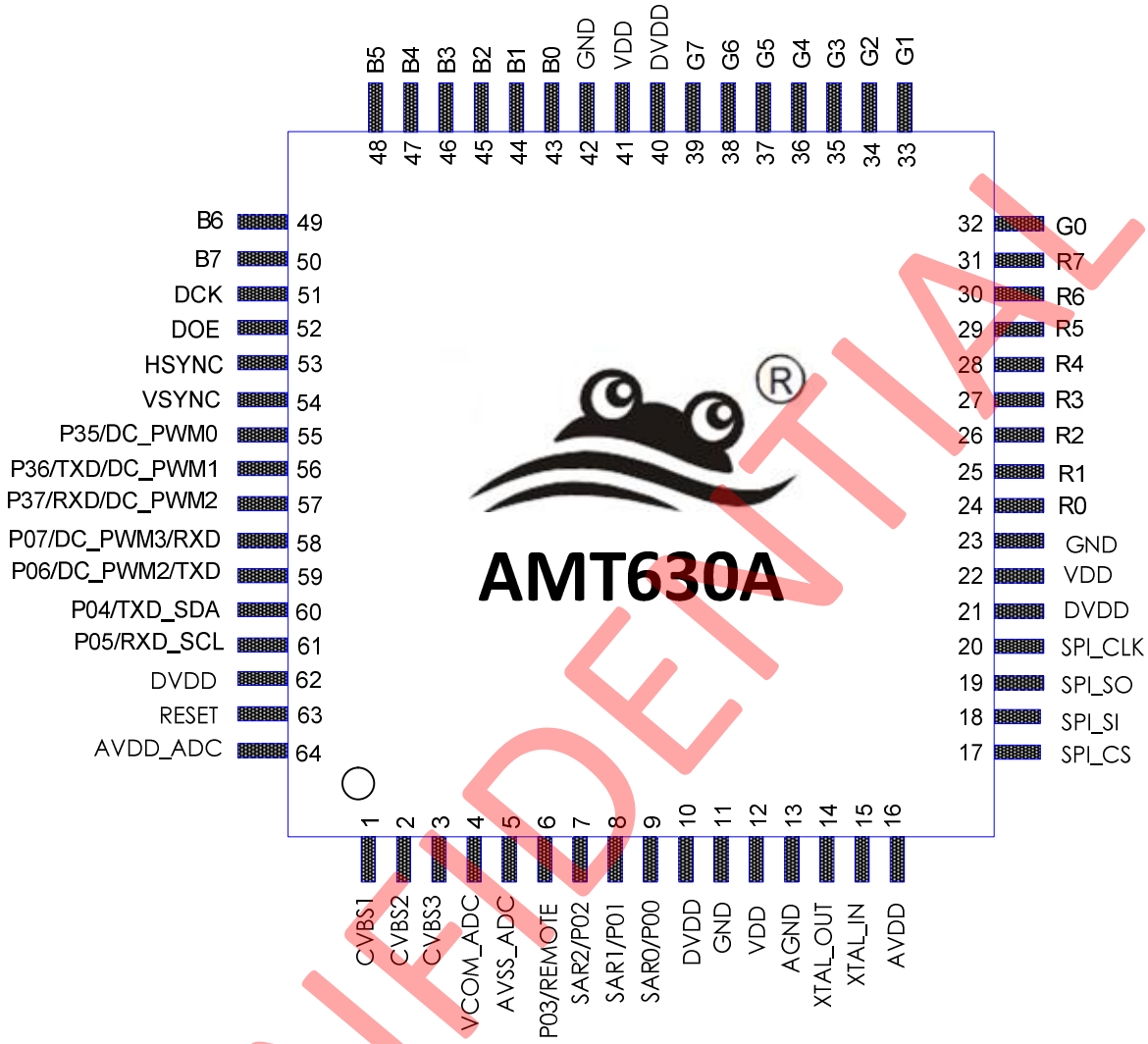
3.1 System apprication diagram



4. Block Diagram



5. Pin Diagram



6. Pin Definition

Pin	TYPE	Function
1	A	CVBS1
2	A	CVBS2
3	A	CVBS3
4	A	VCOM_ADC
5	P	AVSS_ADC (GND)
6	D	P03/REMOTE
7	A	SAR2/P00
8	A	SAR1/P01
9	A	SAR0/P02

10	P	DVDD 3.3V
11	P	GND
12	P	VDD 1.2v (Build-in LDO for 1.2v core power)
13	P	AGND (AVSS33_ANA)
14	A	XTAL_OUT
15	A	XTAL_IN
16	P	AVDD 3.3V
17	D	SPI_CS/P10
18	D	SPI_SI/P11
19	D	SPI_SO/P12
20	D	SPI_CLK/P13
21	P	DVDD 3.3V
22	P	VDD 1.2v (Build-in LDO for 1.2v core power)
23	P	GND
24	D	R0/VOS/tcon_r0/ituVDE/sVSY/cpu_rstn/P14
25	D	R1/HOS/tcon_r1/ituHDE/sHSY/cpu_cs/P15
26	D	R2/DOE/tcon_r2/ituDEO/sDEN/cpu_rs/P16
27	D	R3/DCK/tcon_r3/ituclko/sCLK/cpu_wr/P17
28	D	R4/B7/tcon_r4/itu_d7/sD7/cpu_rd/P20
29	D	R5/B6/tcon_r5/itu_d6/sD6/cpu_d17/P21
30	D	R6/B5/STVR/itu_d5/sD5/cpu_d16/P22
31	D	R7/B4/STVL/itu_d4/sD4/cpu_d15/GPIO0
32	D	G0/B3/tcon_g0/itu_d3/sD3/cpu_d14/GPIO1
33	D	G1/B2/tcon_g1/itu_d2/sD2/cpu_d13/GPIO2
34	D	G2/B1/tcon_g2/itu_d1/sD1/cpu_d12/GPIO3
35	D	G3/B0/tcon_g3/itu_d0/sD0/cpu_d11/GPIO4
36	D	G4/G7/tcon_g4/cpu_d10/P23
37	D	G5/G6/tcon_g5/cpu_d9/P24
38	D	G6/G5/CKV/cpu_d8/P25
39	D	G7/G4/OEV/cpu_d7/P26
40	P	DVDD 3.3V
41	P	VDD 1.2v (Build-in LDO for 1.2v core power)
42	P	GND
43	D	B0/G3/tcon_b0/itu_d0/sD0/cpu_d6/GPIO5
44	D	B1/G2/tcon_b1/itu_d1/sD1/cpu_d5/GPIO6
45	D	B2/G1/tcon_b2/itu_d2/sD2/cpu_d4/GPIO7
46	D	B3/G0/tcon_b3/itu_d3/sD3/cpu_d3/GPIO8
47	D	B4/R7/tcon_b4/itu_d4/sD4/cpu_d2/GPIO9
48	D	B5/R6/tcon_b5/itu_d5/sD5/cpu_d1/GPIO10
49	D	B6/R5/STHR/itu_d6/sD6/cpu_d0/P27
50	D	B7/R4/POL/itu_d7/sD7/cpu_rd/P30
51	D	DCK/R3/tcon_clk/ituclko/sCLK/cpu_wr/P31
52	D	DOE/R2/STHL/ituDEO/sDEN/cpu_rs/P32
53	D	HOS/R1/OEH/ituHDE/sHSY/cpu_cs/P33

54	D	VOS/R0/tck2/ituVDE/sVSY/cpu_rstn/P34
55	D	P35/DC_PWM0
56	D	P36/TXD/DC_PWM1
57	D	P37/RXD/DC_PWM2
58	D	P07/DC_PWM3/RXD
59	D	P06/DC_PWM2/TXD
60	D	P04/TXD/SDA
61	D	P05/RXD/SCL
62	P	DVDD 3.3V
63	D	RESET
64	P	AVDD_ADC 3.3V

7. Electrical Characteristics

7.1 DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DVDD	Digital IO supply voltage		3.0	3.3	3.6	V
I_{DVDD}	Digital supply current		--	40	50	mA
AVDD_ADC	Analog ADC supply voltage		3.0	3.3	3.6	V
I_{AVDD}	Total analog supply current	CVBS input	15	20	30	mA

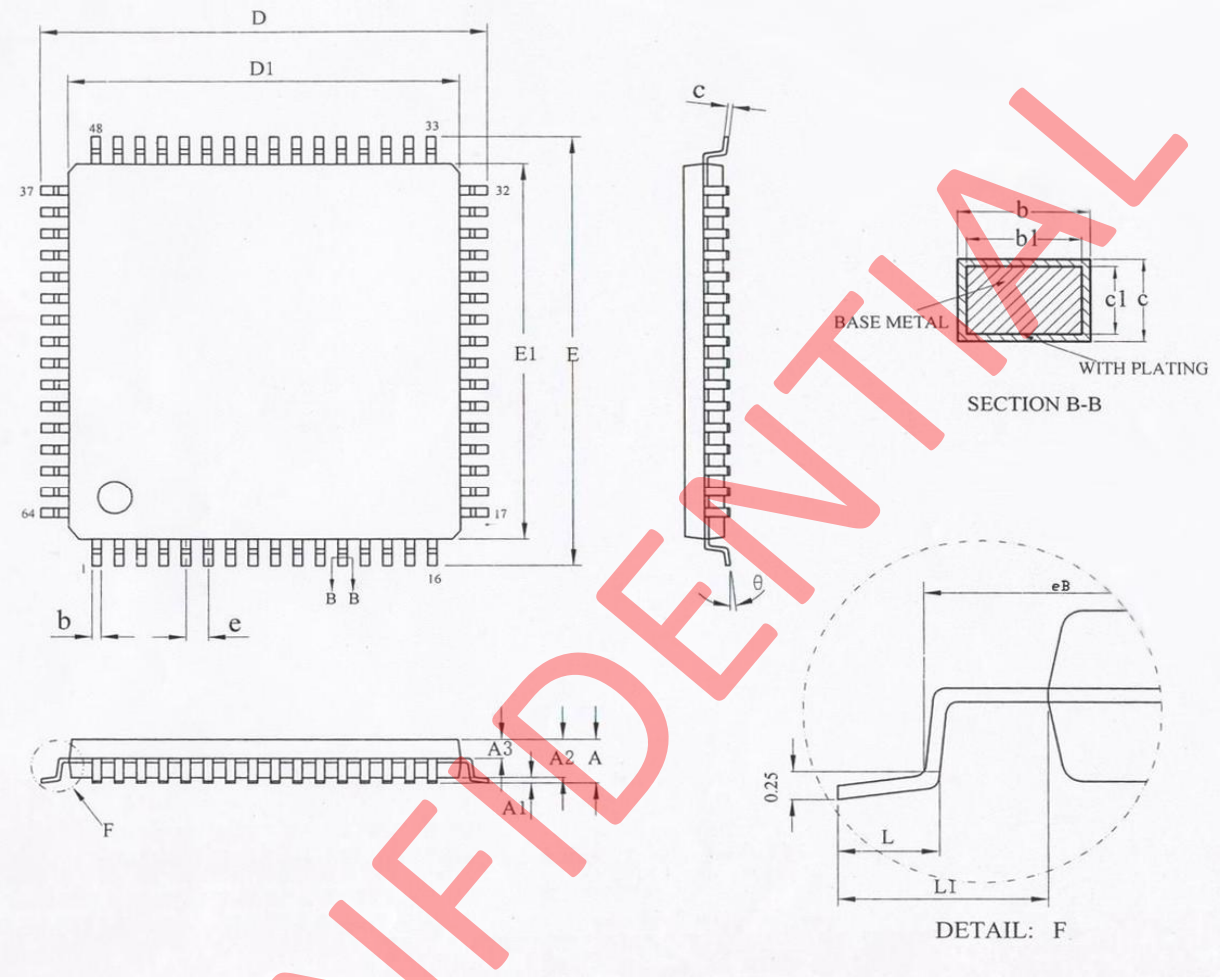
7.2 AC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog part						
Iclamp	Clamping current	VI=1VDC	--	+-16	--	uA
Vi(p_p)	Input voltage (Peak-to-peak value)	For normal video levels 1V(p-p), 3dB termination 18/56 and AC coupling required; Coupling capacitor=22nF	--	2	3.6	V
|Zin|	Input impedance	Clamping current off	200	--	--	KΩ
Ci	Input capacitance		--	--	10	pF
@cs	Channel crosstalk	fi<5MHz	--	--	-50	dB
9-bit analog-to-digital converters						
B	Analog bandwidth	At -3dB	--	7	--	MHz
Φdiff	Differential phase		--	2	--	Deg
Gdiff	Differential gain		--	2	--	%
Fadc	ADC clock frequency		13.5	27	54	MHz
DNL	DC differential linearity Error		--	0.7	--	LSB

INL	DC integral linearity error		--	1	--	LSB
PLL						
FOUT	PLL output range		--	--	500	MHz
FIN	Input reference frequency range		1	--	9	MHz
Fvco	VCO frequency range		--	--	500	MHz
Tjitter	Timing Jitter Peak to Peak		--	88	--	Ps
Tjitter rms	Timing Jitter RMS		--	18	--	Ps
12BIT SAR ADC						
resolution			--	12	--	BIT
Vi(p_p)	input voltage (peak-to-peak value)		--	3.3	3.6	V
Fadc	Sample clock		--	--	1	MHz
INL	DC integral linearity error		--	--	+-2	LSB
DNL	DC differential linearity error		--	--	+-2	LSB
Digital inputs						
VIL(n)	Low-level input voltage		0		0.4	V
VIH(n)	High-level input voltage		2.4		3.6	V
Digital outputs						
VOL	Low-level output voltage		0		0.4	V
VOH	High-level output voltage		2.4		vcc+0.5	V
Temperature						
TA	Ambient Operation Temperature		-20		85	℃
TSTG	Storage Temperature		-40		125	℃
Tj	Junction Temperature				125	℃

8. Package

AMT630A is packaged in a 64 Pin LQFP package.



SYMBOL	MILLIMETER		
	MIN(mm)	NOR(mm)	MAX(mm)
A	-	-	1.60
A1	0.05	-	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.17	-	0.25
b1	0.16	0.18	0.20
c	0.13	-	0.18
c2	0.12	0.127	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10

eB	8.10	-	8.25
e	0.40BSC		
L	0.40	-	0.65
L1	1.00BSC		
θ	0	-	7°
L/F（mil）	160x160		
	210x210		