BM7112 – HD-AHD/TVI / NTSC / PAL Video Decoder with Bi-directional Data Channel

Preliminary Data Sheet

1 Introduction

1.1 Description

BM7112 istheHD/SDvideodecoder supporting High DefinitionTransport Video Interface (HD-AHD/TVI)video decoding as well the legacy NTSC/PAL CVBS video decoding. It can decode any of these input formats from any of the 5 programmable inputs. It also supports differential inputs for the twisted pair wiring application. It works with HD-AHD/TVI encoder for best longdistance HD video transmission. It also canwork with any legacy NTSC/PAL camera for backward compatibility. The primary application is for Automotive HD video or any other applications that require transport of HD video for extended reach.

BM7112 has internal clamping, automatic gain control amplifier for optimal signal conditioning. It has Anti-aliasing filter to reduce crosstalk. Its programmable equalization amplifier and automatic control loop maintain the best performance for low quality and long cable.

BM7112 does majority of the signal processing digitally for its consistency and performance. All control loops are programmable for maximum flexibility. All pixel data are line-locked sampled according to SMPTE-296M and SMPTE-274M standard for the HD-AHD/TVI input. For the NTSC/PAL input, the output is non-standard so as to work together with HD-AHD/TVI format. It has programmable picture control functions for best video quality. Working with AHD encoder and host controller, it supports 2-way data communication through the cable. For the legacy SD signal, it can also provide programmable upstream data support.

The digital video outputs are flexible and compatible with ITU-R BT.1120 interface based on embedded sync. It also support 8-bit output mode at twice the data rate with channel multiplexing capability.

1.2 Features

- Supports 1-CH HD-AHD/TVI 720p/1080p analog HD video decoding
- Supports 1-CH NTSC/PAL CVBS video decoding

Input

- High speed 10-bit Analog-to-Digital converters (ADC) for 2X over-sampling
- Programmable DC restoration or clamp control
- Programmable gain amplifier (PGA) and Automatic Gain Control (AGC) for best S/N performance
- Programmable Anti-aliasing low pass filter
- Embedded Equalizer (EQ) amplifier for best extended reach performance
- Adaptive EQ algorithm for different cable characteristics.
- 5 programmable input multiplexer

Signal Processing

- Brightness, Contrast, Saturation, Hue and Sharpness control through host interface
- Supports SMPTE-296M and SMPTE-274M standard sampling for High Definition signals
- Advanced Sync processor for best low signal performance
- Internal digital Horizontal PLL for Line-Locked sampling

- Internal digital Color PLL for accurate color demodulation
- Color gain control and programmable color killer for best small signal performance
- Internal digital filters for HD Y/C separation
- Integrated high quality adaptive 4H comb filter YC separation for NTSC/PAL decoding to minimize false color and cross luminance artifacts.
- Free run mode with optional blue screen

Output

- ITU-R BT.1120 4:2:2 16-bit outputs with embedded sync.
- Support BT.601 output format with separated H/V sync
- Supports BT.656 compatible Y-C Interleaving output mode per 8-bit VD output channel.
- Flexible output interface

General

- Up-stream data insertion through host interface
- Programmable down-stream data decoding
- Fast 2-wire serial host interface
- Full Power down mode
- Internal PLL for clock generation
- 1.2/3.3V operation
- 48 pin QFN package
- Single 27MHz crystal operation

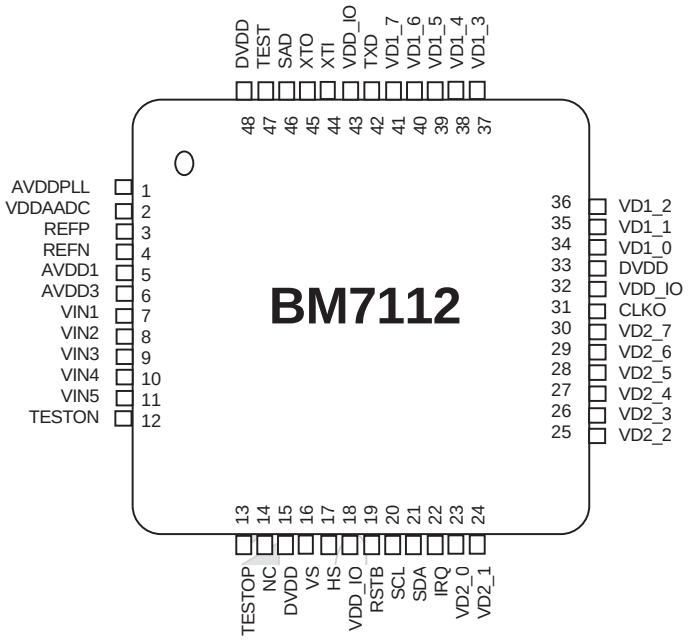
2 Order Information

Package Description

Part #	Name	Description	Pin Count	Body Size	Weight
BM7112JA	QFN 48L	Quad Flat No Lead Package	48	6x6 mm2	0.097g

3 Pin Diagram

48L QFN (Top View)



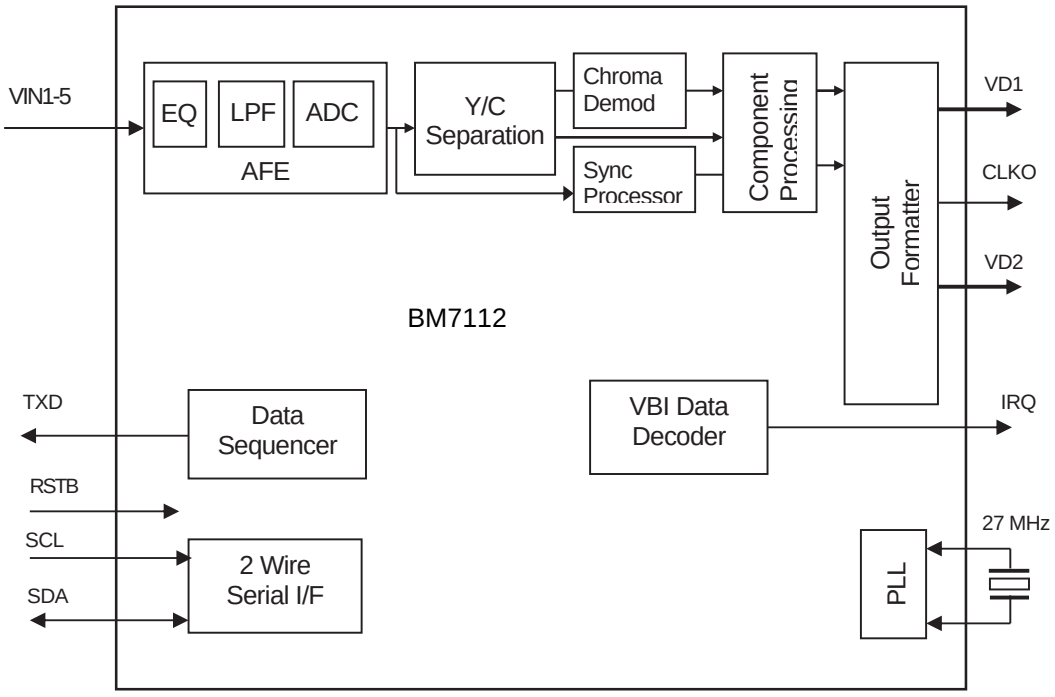
3.1 Pin Description

Pin#	I/O	Pin Name	Description
Analog Section			
7, 8, 9, 10, 11	I	VIN1-5	Analog Video input. The signal should be AC coupled in by 0.1uF. Unused inputs should be connected to AVSS through 0.1uF.
3	I	REFP	ADC positive reference. Connect 0.1uF to AVDD and REFP
4	I	REFN	ADC negative reference. Connect 0.1uF to Ground and REFN
2, 5	P	VDDAADC, AVDD1	Analog 1.2V power supply
6	P	AVDD3	Analog 3.3V power supply
1	P	AVDDPLL	Analog 3.3V PLL power supply
12, 13	O	TSTON, TSTOP	Analog Test Pins. Unconnected during normal operation
Digital Section			
41, 40, 39, 38, 37, 36, 35, 34	O	VD1_7-0	VD1 data output
31	O	CLKO	CH1 clock output at 74.25 or 148.5 MHz
30, 29, 28, 27, 26, 25, 24, 23	O	VD2_7-0	VD2 data output
16	O	VS	Vertical Sync
17	O	HS	Horizontal Sync
44	I	XTI	Crystal Input or clock input
45	O	XTO	Crystal output
46	I	SAD	The MPU Serial interface Chip Address Select
20	I	SCL	The MPU Serial interface Clock Line
21	B	SDA	The MPU Serial interface Data Line
19	I	RSTB	Reset input. Low active
22	O	IRQ	Interrupt signal output
42	O	TXD	Up stream data signal output. Unconnected when not used.
47	I	TEST	Test pin (Connect to VSS for normal operation)
18, 32, 43	P	VDD_IO	Digital 3.3V power supply
15, 33, 48	P	DVDD	Digital 1.2V power supply
14	-	NC	

I = Input, O=Output, B=Bidirectional, P=Power

4 Functional Description

4.1 Block Diagram



5 Parametric Information

5.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
AVDD3, AVDDPLL to Ground	-	**-0.5**	-	4.0	V
AVDD1 to Ground		**-0.5**	-	1.6	V
DVDD to Ground	-	**-0.5**	-	1.6	V
VDD_IO to Ground	-	**-0.5**	-	4.0	V
Digital Signal Input Pin to Ground	-	-0.5	-	VDD_IO+ 0.5	V
Analog Input Voltage	-	Ground – 0.5	-	1.92	V
Storage Temperature	T_S	–65	-	+150	°C
Junction Temperature	T_J	-	-	+125	°C
Vapor Phase Soldering (15 Seconds)	T_{VSOL}	-	-	+220	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the ranges list in above table can induce

5.2 Recommended Operation Condition

5.2.1 Power Supply

Parameter	Symbol	Min	Typ	Max	Units
Power Supply — IO	V_{DD_IO}	3.15	3.3	3.45	V
Power Supply — Analog 3.3V	AVDD3	3.15	3.3	3.45	V
Power Supply — Analog 1.2V	AVDD1	1.1	1.2	1.3	V
Power Supply — Digital	DVDD	1.1	1.2	1.3	V
Maximum $\|V_{DD\_IO} -$ AVDD$\|$		-	-	0.3	V
Ambient Operating Temperature	T_A	-40		+85	°C

5.2.2 Reference Clock Input

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DD_IO} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input Clock Frequency	Fclk		27		MHz
Crystal Spec					

Nominal frequency (fundamental)		-	27	-	MHz
Deviation base on normal operation condition		-50	-	+50	ppm
Load capacitance	CL	-	20	-	pF
Series resistor	RS	-	80	-	Ohm
Oscillator Input					
Nominal frequency		-	27	74.25	MHz
Deviation		-50	-	+50	ppm
Duty cycle		-	-	55	%

5.3 AC/DC Characteristic

5.3.1 Power Consumption

Parameter	Symbol	Min	Typ	Max	Units
Analog Supply current (3.3V) AFE	Iaa3	-	20	23	mA
PLL		-	4	-	mA
Analog supply current (1.2V)	Iaa12		100	132	mA
Digital I/O Supply current 1080p 8-b	Idde	-	53		mA
1080p 16-b			23		
720p 30 / CVBS 8-b			28		
720p 30 / CVBS 16-b			15		
Digital Core Supply Current 1080p	Idd	-	72	86	mA
720p /	CVBS		36	46	

5.3.2 DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	-	-	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DD_IO} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input High Current (V_{IN} =V_{DD})	I_{IH}	-	-	10	μA
Input Low Current (V_{IN} =VSS)	I_{IL}	-	-	–10	μA
Input Capacitance (f=1 MHz, V_{IN} =2.4 V)	C_{IN}	-	5	-	pF
Digital Outputs					
Output High Voltage (I_{OH} = –12 mA)	V_{OH}	2.4	-	V_{DD_IO}	V
Output Low Voltage (I_{OL} = 12 mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	μA
Output Capacitance	C_O	-	5	-	pF

5.3.3 Analog Electrical Characteristics

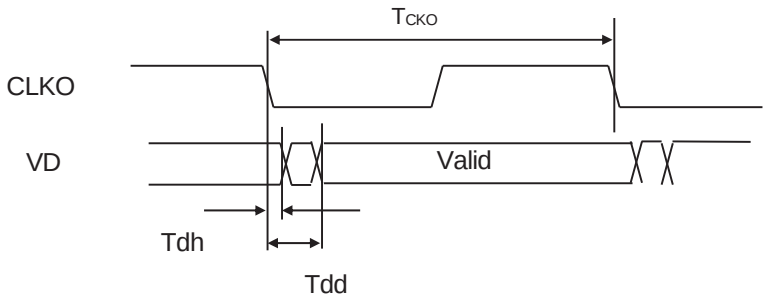
Parameter	Symbol	Min	Typ	Max	Units
Analog Input					
Analog Pin Input voltage	Vi	0.5	1	1.5	Vpp
Analog Pin Input Capacitance	C A	-	7	-	pF
ADCs					
ADC resolution	ADCR	-	10	-	bits
ADC integral Non-linearity	AINL	-	±1	-	LSB
ADC differential non-linearity	ADNL	-	±1	-	LSB
ADC clock rate	f_{ADC}	-	-	160	MHz
Video bandwidth (-3db)	BW	-	70	-	MHz

5.3.4 Decoder Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Horizontal PLL					
Line frequency	f_{LN}	15.625		45	KHz
static deviation	Δf_H	-	-	6.2	%
Vertical PLL					
Frame/Field frequency	f_{LN}	15		60	KHz
static deviation	Δf_H	-	-	5.5	%
Subcarrier PLL					
Lock in range (SPR=0) – HD 1080p, 720p60/50	Δf_{S-HD}	-		±4500	Hz
Lock in range (SPR=0) – HD 720p30/25	Δf_{S-HD}	-		±2200	Hz
Lock in range (SPR=2) - SD	Δf_{S-SD}	-		±800	Hz

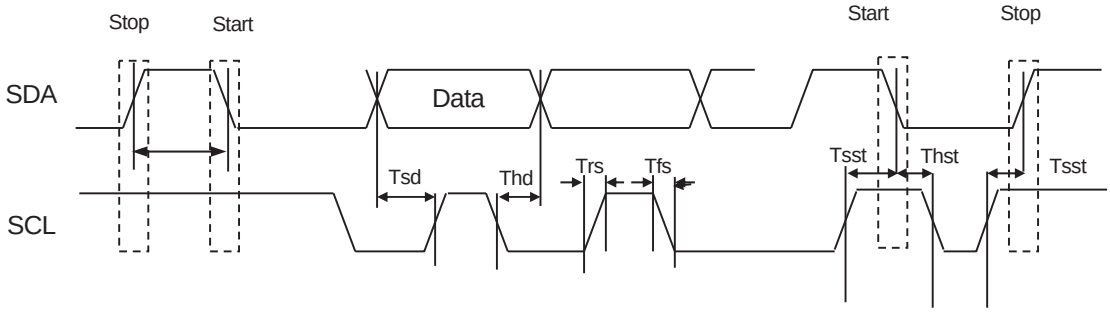
5.3.5 Clocks, Data Timing

Parameter	Symbol	Min	Typ	Max	Units
Output CLKO					
Frequency (1/ T_{CKO})	F_{CKO}	-		148.5	MHz
Duty Cycle		-	-	55	%
Rise/Fall time (12mA)		1	1.5		ns
CLKO (Falling Edge) to Data Delay @ 74.25MHz	Tdd	-	1.8	2.2	ns
CLKO (Falling Edge) to Data Delay @ 148.5MHz	Tdd	-	1.6	1.8	ns
Data hold time	Tdh	-	0	-	ns



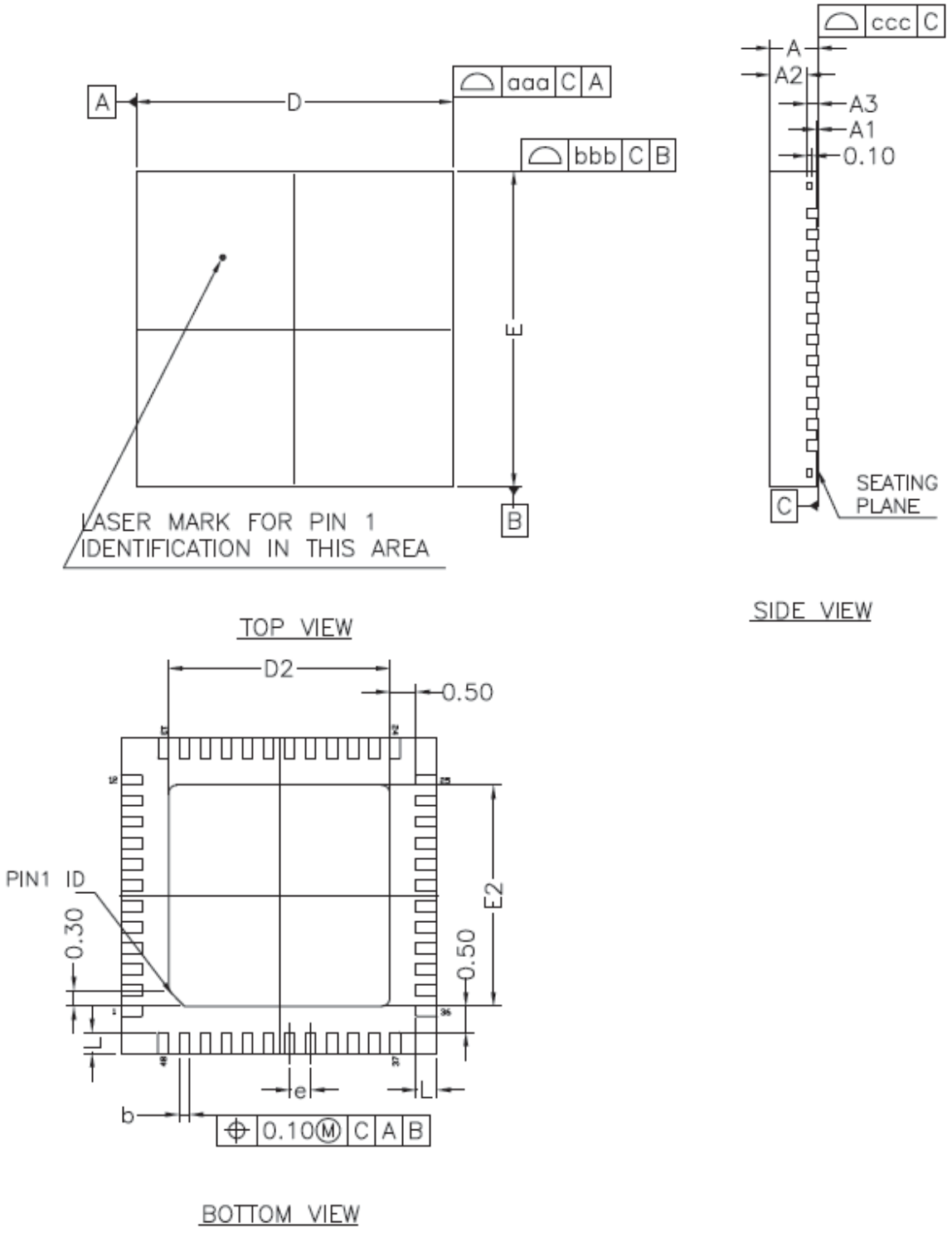
5.3.6 Serial Interface Timing

Parameter	Symbol			Min	
Setup time for start/stop condition	Tsst	200			ns
Hold time for start / stop condition	Thst	200			ns
Data setup time (write)	Tsd	100			ns
Data hold time (write)	Thd(w)	100	-		ns
SCL, SDA rise time	Trs	250			ns
SCL, SDA rise time	Tfs	250			ns
SCL (Falling edge) to SDA delay time (read)	Thd(r)	150			ns
SCL clock frequency	fscl	-	400	1000	KHz



6 Mechanical Data

6.1 48 Pin QFN



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.035	0.05	0.000	0.001	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.00 bsc			0.236 bsc		
D2	4.10	4.20	4.30	0.161	0.165	0.169
E	6.00 bsc			0.236 bsc		
E2	4.10	4.20	4.30	0.161	0.165	0.169
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.40 bsc			0.016 bsc		
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.08			0.003		

2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.

7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF